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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,462	06/26/2003	Scott L. Michaelis	200205355-1	3496

22879 7590 01/18/2008

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ART UNIT	**PAPER NUMBER**
2116	

NOTIFICATION DATE	DELIVERY MODE
01/18/2008	ELECTRONIC

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/606,462
Filing Date: June 26, 2003
Appellant(s): MICHAELIS ET AL.

Craig J. Cox (Reg. No. 39,643)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed November 9, 2007 appealing from the Office action mailed May 3, 2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

7,103,639 B2	Walton et al.	09-2006
2003/0236972 A1	Harrington et al.	12-2003

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 15-20 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Walton et al. (U.S. Patent No. 7,103,639 B2) (hereinafter referred to as Walton).

As to claim 15, Walton discloses a partition of multiple partition computer system comprising: a plurality of processors (CPUs 302); firmware (PDH) comprising a reset code that resets a portion (cell) of the partition, wherein one processor of the plurality of processors ("monarch" processor) executes the reset code (Walton discloses the "monarch" processor within a cell managing booting and processor formation wherein PDH is a firmware device comprising

booting code which is inclusive of initialization and reset; column 3, lines 5-12 and column 5, lines 35-47); and random access memory (cache within CM 304) that is not affected by the reset code, that stores a list of addresses associated with the portion (Walton discloses a complex profile being created which is a "map" of the cell configuration which comprises location of devices assigned to a cell/partition which inherently would contain processor locations [addresses] and therefore register addresses; column 2, lines 7-15 and column 4, line 47 thru column 5, line 34).

As to claim 16, Walton further discloses the partition of claim 15, further comprising: read only memory that stores the firmware (column 3, lines 5-12).

As to claim 17, Walton further discloses the partition of claim 15, further comprising: a plurality of cells (see Fig. 1); wherein each cell comprises at least one processor of the plurality of processors (CPUs 302), and each cell comprises a reset register (state register) having an address that is on the list (column 5, line 55 thru column 6, line 20).

As to claims 18-20, they are directed to the partition of steps set forth in claim 17. Therefore, they are rejected for the same basis as set forth hereinabove.

As to claim 23, Walton disclose a computer readable medium having computer program logic recorded thereon for operating a partition of a multiple partition computer system, wherein the partition comprises a plurality of processors (CPUS 301), the computer program logic comprising: means for (101) building a list (data structure called complex profile) of reset register addresses associated with the plurality of processors (Walton discloses a complex profile being created which is a "map" of the cell configuration which comprises location of devices assigned to a cell/partition which inherently would contain processor

locations [addresses] and therefore register addresses; column 2, lines 7-15 and column 4, line 47 thru column 5, line 34); means for (state registers via CM 304) placing each processor of the plurality of processors into a known state (column 4, lines 47-63 and column 5, line 55 thru column 6, line 6); and, means for (CM 304) resetting the plurality of processors by writing a reset code (BIB) into their associated reset registers (column 4, lines 47-63 and column 5, line 55 thru column 6, line 20).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walton (as cited above) in view of Harrington et al. (U.S. Patent Publication No. 2003/0236972 A1) (hereinafter referred to as Harrington).

As to claim 1, Walton discloses a method for resetting a partition of a multiple partition system, wherein the partition (see Fig. 1) comprises a plurality of processors (CPUs 302), the method comprising: executing, by one processor ("monarch" processor) of the plurality of processors, a reset code from firmware (PDH module) (Walton discloses the "monarch" processor within a cell managing booting and processor formation wherein PDH is a firmware device comprising booting code which is inclusive of initialization and reset; column 3, lines 5-12 and column 5, lines 35-47); building a list (data structure called complex profile) of reset

register addresses associated with the plurality of processors (Walton discloses a complex profile being created which is a "map" of the cell configuration which comprises location of devices assigned to a cell/partition which inherently would contain processor locations [addresses] and therefore register addresses; column 2, lines 7-15 and column 4, line 47 thru column 5, line 34); sending an interrupt (step 206 or 208) to the other processors of the plurality of processors (Walton discloses step 206 of Fig. 2 resetting a cell which necessitates an interrupt to the other processors of the cell upon reset. Also, Walton discloses the system "synchronizing" of cells in step 208 in Figs. 2 and 3 which also necessitates an interrupt; column 6, line 47 thru column 7, line 11); resetting the other processors (via CM 304) by writing a reset code to their associated reset registers (state register(s) associated with the cells) (column 4, lines 47-63 and column 5, line 55 thru column 6, line 20).

Walton fails to explicitly disclose resetting the one processor by writing to its associated reset register.

Harrington teaches a partitioned system wherein one processor of the partition (step 520 of Fig. 5) to process a warm reboot request (which sends out reset signals and interrupts to all of the other partition processors; paragraph 23 and paragraph 12) and then pass the control over to a service processor (135) to reset *all* of the processors in the partition and continue with the warm reboot (paragraphs 51 and 52). Therefore, the "one processor" of the partition resets all of the other processors and then a service processor (135) resets all of the processors to include the "one processor." Walton also teaches the system creating a list of resources (locating the resources) which is maintained by the system firmware (paragraph 4). Walton has the additional

benefit of having a more reliable reboot process in a partition system ensuring all pending I/O requests within the system are halted/completed (paragraphs 12 and 13).

It would have been obvious to one of ordinary skill of the art having the teachings of Walton and Harrington at the time the invention was made, to modify method of Walton to include the step of resetting the one processor as taught by Harrington. One of ordinary skill in the art would be motivated to make this combination of including the step of resetting the one processor after resetting all of the other processors in the partition in view of the teachings of Harrington, as doing so would give the added benefit of having a more reliable reboot process in a partition system ensuring all pending I/O requests within the system are halted/completed (as taught by Harrington above).

As to claim 2, Walton in combination with Harrington taught the method in claim 1, as shown above. Walton further teaches the method further comprising: storing the firmware on a read only memory (column 3, lines 5-12).

As to claim 3, Walton in combination with Harrington taught the method in claim 1, as shown above. Walton further teaches the method further comprising: storing the list of reset register addresses in random access memory ("caching" the complex profile within the CM 304; column 4, line 47 thru column 5, line 34).

As to claim 5, Walton in combination with Harrington taught the method in claim 1, as shown above. Harrington further teaches the method further comprising: requesting the execution of the reset code by a processor of the plurality of processors (paragraph 50).

As to claim 6, Walton in combination with Harrington taught the method in claim 1, as shown above. Harrington further teaches the method further comprising: requesting the

execution of the reset code by an operating system of the multiple partition system (paragraphs 50 and 51).

As to claim 7, Walton in combination with Harrington taught the method in claim 1, as shown above. Harrington further teaches the method further comprising: requesting the execution of the reset code by a firmware shell (hypervisor) of the multiple partition system (RTAS of hypervisor; paragraphs 42, 45 and 50).

As to claim 9, Walton in combination with Harrington taught the method in claim 1, as shown above. Harrington further teaches the method further comprising: flushing a cache associated with the one processor, after sending the interrupt (resetting all of the processors in the partition after running RTAS necessitates flushing the cache of the one processor; paragraphs 23, 50 and 51).

As to claim 10, Walton in combination with Harrington taught the method in claim 1, as shown above. Harrington further teaches the method further comprising: moving execution from main memory to read only memory (from the operating system to the hypervisor; paragraph 51).

As to claim 12, Walton in combination with Harrington taught the method in claim 1, as shown above. Walton further teaches the method wherein the partition comprises a plurality of cells, and each cell comprises at least one processor, the method further comprises: inventorying (updating the complex profile) the plurality of cells for resetting (column 5, lines 23-34).

As to claim 13, Walton in combination with Harrington taught the method in claim 1, as shown above. Walton further teaches the method wherein resetting the one processor occurs after resetting the other processors (paragraphs 50 and 51).

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Walton and Harrington as applied to claim 1 above, and further in view of Applicant's Admitted Prior Art (hereinafter referred to as AAPA).

Applicant has admitted in the Background of the Invention that cells in a partition include Itanium Processor Family chips (paragraph 2).

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Walton as applied to claim 15 above, and further in view of Harrington (as cited above).

As to claims 21, Walton fails to explicitly disclose the partition wherein the one processor is reset after the other processors of the plurality of processors are reset.

Harrington teaches a partitioned system wherein one processor of the partition (step 520 of Fig. 5) to process a warm reboot request (which sends out reset signals and interrupts to all of the other partition processors; paragraph 23 and paragraph 12) and then pass the control over to a service processor (135) to reset *all* of the processors in the partition and continue with the warm reboot (paragraphs 51 and 52). Therefore, the "one processor" of the partition resets all of the other processors and then a service processor (135) resets all of the processors to include the "one processor." Walton also teaches the system creating a list of resources (locating the resources) which is maintained by the system firmware (paragraph 4). Walton has the additional benefit of having a more reliable reboot process in a partition system ensuring all pending I/O requests within the system are halted/completed (paragraphs 12 and 13).

It would have been obvious to one of ordinary skill of the art having the teachings of Walton and Harrington at the time the invention was made, to modify method of Walton to include the step of resetting the one processor as taught by Harrington. One of ordinary skill in

the art would be motivated to make this combination of including the step of resetting the one processor after resetting all of the other processors in the partition in view of the teachings of Harrington, as doing so would give the added benefit of having a more reliable reboot process in a partition system ensuring all pending I/O requests within the system are halted/completed (as taught by Harrington above).

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Walton as applied to claim 15 above, and further in view of Applicant's Admitted Prior Art (hereinafter referred to as AAPA).

Applicant has admitted in the Background of the Invention that cells in a partition include Itanium Processor Family chips (paragraph 2).

(10) Response to Argument

A. First Ground of Rejection

Claims 15-20 and 23 are rejected under 35 USC § 102(b) as being anticipated by Walton.

Claims 15-19

As to claim 15, Appellant argues that nowhere does Walton disclose a firmware comprising a reset code that resets a portion of a partition and random access memory that is not affected by the reset code, that stores a list associated with the portion. The Examiner disagrees.

First in claim 15, Walton discloses a multiple partition system that comprises a processor dependent hardware module (firmware) that is used to boot and reset a system (column 3, lines 5-12). The resetting (as depicted in step 204, 206, 211 or 214 of Fig. 2) of a cell (portion of a partition) is carried out by a monarch processor (one processor) that is responsible for utilizing

the firmware within the partition to reset the cell when needed (column 5, lines 38-47). Therefore, Walton clearly anticipates *a firmware* (processor dependent hardware module) *comprising a reset code* (as shown in column 3, lines 5-12) *that resets a portion of a partition* (and column 5, lines 38-47).

Furthermore in re claim 15, Walton continues to disclose cell microcontrollers that comprise caches (random access memory) to store a data structure referred to as a complex profile (column 5, lines 23-31). The complex profile is a "map" that is created by a service processor module when the cell is booted or reset (column 4, line 51 thru column 5, line 4). This "map" is a data structure that describes the entire partition complex structure such that all partitions, cells of partitions and the processors of the cells are mapped which inherently necessitates a list associated with the cell (portion of the partition). Therefore, Walton clearly anticipates a *random access memory* (caches of the cell microcontrollers) *that is not affected by the reset code, that stores a list* (map of the complex) *associated with the portion* (cell) that is comprised of multiple processors.

Therefore, claim 15 stands rejected under 35 USC § 102(b) as anticipated by Walton for the reasons argued above. As a result, dependent claims 16-19 remain rejected based on dependence to independent claim 15 as well as the reasons argued under **(9) Grounds of Rejection**.

Claim 20

The limitations for the structure of the partition comprising a plurality of cells can be found in Walton (at column 2, line 50 thru column 3, line 22) that describes an entire *complex* comprising *multiple partitions* wherein each partition is comprised of portions of partitions

described as *cells* that is comprised of multiple processors. The "one processor" (microcontrollers CM 304) and the processor address locations (stored in the "complex profile") is the already described herein above. Therefore, claims 17 and 20 stand rejected under 35 USC § 102(b) as anticipated by Walton for the reasons argued above.

Claim 23

As to claim 23, the means for "building a list" of reset register addresses is argued herein above such that the arguments presented for storing a list associated with the portion claim 15 describes the entire structure (map) built when booting or resetting a portion of a partition. The "map" of the complex (complex profile) inherently necessitates storing addresses of the reset registers since this structure description is used to know the locations via the map.

Furthermore in re claim 23, Appellant argues that Walton does not disclose placing each processor of the plurality of processors into a known state. The Examiner disagrees. Walton discloses (at step 208a of Fig. 3) synchronizing all of the processors before resetting by waiting for said processors to get a to RENDEZ state before starting (column 6, line 60 thru column 7, line 11).

As to the "writing a reset code into their [processors] associated reset registers," this limitation is inherently necessitated to reset a PC family (Intel, IBM, AMD, etc.) processor.

Therefore, claim 23 stands rejected under 35 USC § 102(b) as anticipated by Walton for the reasons argued above.

B. Second Ground of Rejection

Claims 1-13 are rejected under 35 USC § 103(a) over Walton in view of Harrington.

Claims 1-3, 5-7, 9-10 and 12

As to claim 1, the Appellant argues that neither Walton nor Harrington teaches executing by one processor of the plurality of processors, a reset code from firmware, building a list of reset register addresses associated with the plurality of processors, sending an interrupt to the other processors of the plurality of processors, resetting the other processors by writing a reset code to their associated reset registers, and resetting the one processor by writing to its associated reset register. The Examiner disagrees.

The limitations of *executing by one processor of the plurality of processors, a reset code from firmware, building a list of reset register addresses associated with the plurality of processors, sending an interrupt to the other processors of the plurality of processors, resetting the other processors by writing a reset code to their associated reset registers* are all argued herein above in re independent claims 15 and 23. Therefore, these limitations *are disclosed* by Walton for the reasons argued above.

As to the limitation of *resetting the one processor by writing to its associated reset register*, the Harrington reference is used. Harrington describes a partition system wherein a partition is reset (paragraphs 12, 23 and 51). After all of the processors are reset in the partition by a service processor (one processor), the service processor is reset by a partition manager (paragraph 51). Therefore, Harrington teaches *resetting the one processor* (service processor) *by writing to its associated reset register* (via partition manager).

Therefore, claim 1 stands rejected under 35 USC § 103(a) over Walton in view of Harrington for the reasons argued above. As a result, claims 2, 3, 5-7, 9-10 and 12 are rejected based on dependence to independent claim 1 as well as the reasons argued under **(9) Grounds of Rejection**.

Lack of Motivation

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, motivation to combine was suggested in Harrington at paragraphs 12 and 13.

C. Third Ground of Rejection

Claims 14 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Walton and Harrington as applied to claim 1 above, and further in view of AAPA. However, claim 14 stands rejected based on dependence to independent claim 1 as well as the reasons argued under **(9) Grounds of Rejection**.

D. Fourth Ground of Rejection

Claims 21 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Walton as applied to claim 15 above, and further in view of Harrington. However, claim 21 stands rejected based on dependence to independent claim 15 as well as the reasons argued under **(9) Grounds of Rejection**.

E. Fifth Ground of Rejection

Claims 22 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Walton as applied to claim 15 above, and further in view of AAPA. However, claim 22 stands rejected

based on dependence to independent claim 15 as well as the reasons argued under **(9) Grounds of Rejection.**

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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Patent Examiner
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1/10/2008

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